of the pullup resistor is unimportant, but, for best speed, it should be as small as practical to reduce the RC change time of the output signal of the 74LVC2G07. The current output of the74LVC07A is 24 mA at 3.3V; at that V_{CC}, the pullup resistor could be as low as 150Ω. It should be as large as possible to reduce power consumption.

The 74LVC2G07 supply level determines V_{OL} and V_{OH} at B. At 1.8V, the V_{OH} would be near V_{CC}, and V_{OL} is 0.45V or lower when driving a 4-mA load. The 74LVC2G07 and 74LVC2G241 provide a quick and easy way to obtain a bidirectional level translation and take up little board space.□

Simple nanosecond-width pulse generator provides high performance

Jim Williams, Linear Technology Corp

If you need to produce extremely fast pulses in response to an input and trigger, such as for sampling applications, the predictably programmable short-time-interval generator has broad uses. The circuit of **Figure 1**, built around a quad high-speed comparator and a high-speed gate, has settable 0- to 10-nsec output width with 520-psec, 5V transitions. Pulse width varies less than 100 psec with 5V supply variations of 65%. The minimum input-trigger width is 30 nsec, and input-output delay is 18 nsec.

Comparator IC_1 inverts the input pulse (Figure 2, Trace A) and isolates the 50Ω termination. IC_1's output drives fixed and variable RC networks. Programming resistor R_G primarily determines the networks' charge-time difference and, hence, delay at a scale factor of approx 80Ω/nsec.

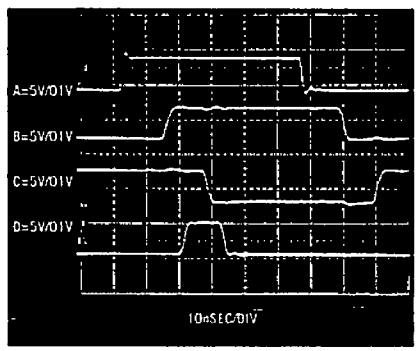

Figure 2 Pulse-generator waveforms, viewed in 400-MHz real-time bandwidth, include input (Trace A), IC_3 (Trace B) fixed and IC_2 (Trace C) variable outputs and output pulse (Trace D). RC networks differential delay manifests as IC_2-IC_3 positive overlap. G_1 extracts this interval and presents circuit output.

Comparators IC_2 and IC_3, arranged as complementary-output-level detectors, represent the networks' delay difference as edge-timing skew. Trace B is IC_3's fixed-path output, and Trace C is IC_2's variable output. Gate G_1's output (Trace D), which is high during IC_2-IC_3 positive overlap, presents the circuit output pulse. **Figure 2** shows a 5V, 5-nsec width, measured at 50% amplitude, output pulse with R=390Ω. The pulse is clean and has well-defined transitions. Post-transition aberrations, within 8%, derive from G_1's bond-wire inductance and an imperfect

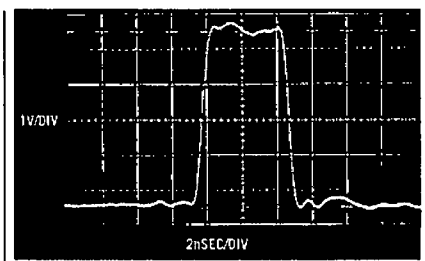

Figure 3 The 5-nsec-wide output with R=390Ω is clean with well-defined transitions. Post-transition aberrations are within 8% and derive from G_1 bond-wire inductance and an imperfect coaxial probe path.

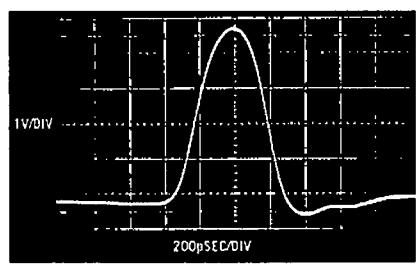

Figure 4 The narrowest amplitude pulse width is 1 nsec, and the base width measures 1.7 nsec. Measurement bandwidth is 3.9 GHz.

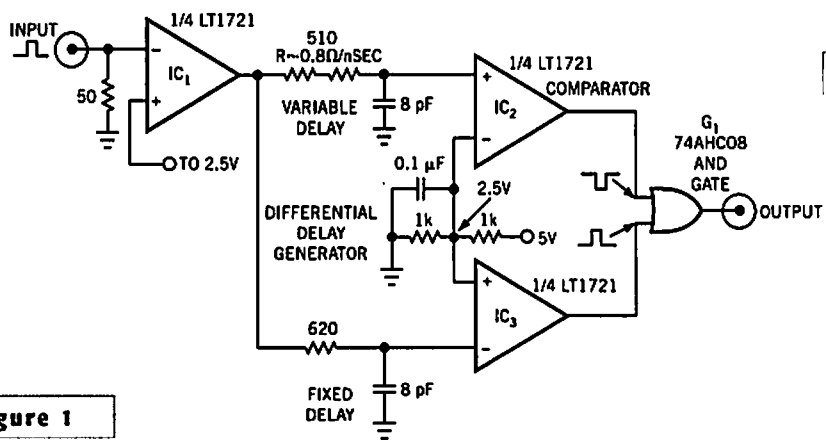

Figure 1 This pulse generator has 0- to 10-nsec width and 520-psec transitions. IC_1 unloads termination and drives the differential delay network. The IC_2-IC_3 complementary outputs represent delay difference as edge timing skew. G_1, which is high during IC_2-IC_3's positive overlap, presents circuit output.

coaxial probing path. Figure 3 shows the narrowest full amplitude, 5V pulse available. Width measures 1 nsec at the 50% amplitude point and 1.7 nsec at the base in a 3.9-GHz bandwidth. Shorter widths are available if partial amplitude pulses are acceptable. Figure 4 shows a 3.3V, 700-psec width (50%) with a 1.25-nsec base. G_1's rise time limits minimum achievable pulse width. The partial-amplitude pulse, 3.3V high, measures 700 psec with a 1.25-nsec base (Figure 5). Figure 6, taken in a 3.9-GHz sampled bandpass, measures 520-psec rise time. Fall time is similar. The transition of the probe edge is well-defined and free of artifacts.□

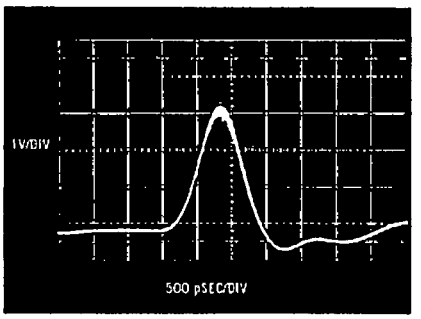

Figure 5 The partial-amplitude pulse, 3.3V high, measures 700 psec wide with a 1.25-nsec base. The trace granularity is an artifact of the 3.9-GHz-sampling-oscilloscope operation.

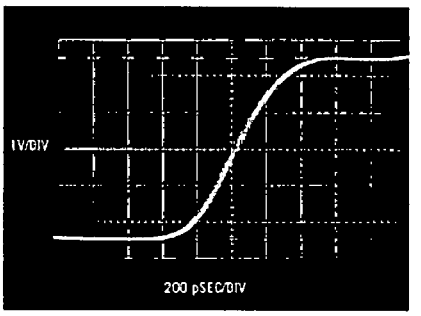

Figure 6 A transition detail in the 3.9-GHz bandpass with rise time of 90 psec shows 520-psec rise time; fall time is similar. The granularity derives from sampling-oscilloscope operation.

Accurately measure resistance with less-than-perfect components

Dave Van Ess, Cypress Semiconductor

FOR TRANSDUCERS, such as strain gauges or thermistors, you must accurately and inexpensively measure resistance using circuitry built with imperfect components and in which gain and offset errors can significantly limit the accuracy of ohmic measurements. The right circuit topology makes it possible to eliminate most error terms while measuring ohms, leaving the accuracy to be determined by just a single reference resistor.

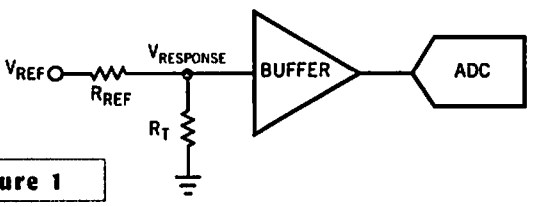

Figure 1 The resistive-divider topology provides a lower cost alternative to a current source and a precision resistor for calibration.

Unlike measuring voltage or current, measuring a passive attribute, such as resistance, requires a stimulus. One method of measuring resistance is to force a known current through a resistor and measure the voltage across the resistor. Measuring ohms in this way means that, with the correct selection of stimulus current, you need do no math, so this method was popular when the cost of computation was more than the cost of building an accurate current source. However, the accuracy of the current source directly limits the accuracy of the reading and any gain or offset errors from measuring the response voltage offsets the accuracy, as well. Additionally, the range of measurement is limited to the ADC's signal range, as the following equation shows:

$$R_T(MAX) = \frac{V_{RESPONSE}(MAX)}{I_{STIM}}.$$

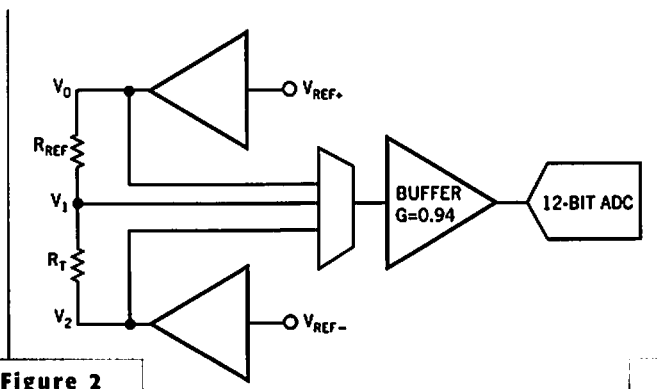

Figure 2 Remove most gain and offset errors using two measurements and a ratio calculation.

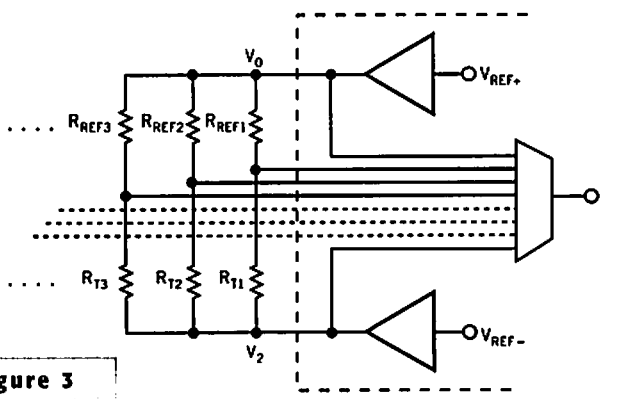

Figure 3 Extend the idea to handle multiple sensors and signal paths, using multiplexing through a single buffer and A/D converter.